AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions, and listings, of claims in the application.

1. (Previously presented) An arrangement for performing Viterbi decoding using a trellis, which the arrangement comprises one or more Add, Compare, Select ("ACS") units, wherein connections between the inputs and outputs of the ACS units are implemented in such a manner that in calculating consecutive metrics of the trellis, the calculated metrics of the previous stage of the trellis obtained from the outputs of the ACS units are directly connected to the inputs of the ACS units to be used in the calculation of the next stage of the trellis and the arrangement further comprises a memory for storing the calculation results and that the connections between the inputs and outputs of the ACS units are implemented in such a manner that $\log_Y P$ path metrics are calculated per one memory read/write operation pair, wherein P is the number of data paths and Y is the number of branches from/to a state.

2. (Canceled)

3. (Previously presented) The arrangement as claimed in claim 1, wherein the ACS units are arranged to calculate Y ACS operations each, wherein Y is the number of branches from/to a state.

4. (Previously presented) The arrangement as claimed in claim 1, wherein the arrangement comprises ACS banks made up of several ACS units.

5. (Previously presented) The arrangement as claimed in claim 4, wherein the arrangement comprises ACS banks in a cascade connection.

6. (Previously presented) The arrangement as claimed in claim 4, wherein the arrangement comprises ACS banks in a parallel connection.

7. (Previously presented) The arrangement as claimed in claim 4, wherein the output of the ACS bank used in the calculation is connectable back to the input of the bank.

8. (Previously presented) The arrangement as claimed in claim 4, wherein the ACS bank is implemented by program in a processor.

9. (Previously presented) The arrangement as claimed in claim 8, wherein the processor is arranged to store the calculated metrics of a previous stage of the trellis into a register and to read the stored metrics from the register when calculating the metrics of the next stage of the trellis.

10. (Currently amended) A method for performing Viterbi decoding using a trellis, comprising:

calculating by one or more Add, Compare, Select ("ACS") units a set of consecutive metrics of the trellis using metrics of a previous stage of the trellis calculated by one or more ACS units directly as input; [[and]]

storing the calculation results into a memory and calculating $\log_Y P$ path metrics per one memory read/write operation pair, wherein P is the number of data paths and Y is the number of branches from/to a state; and

generating decoded data based upon the calculated set of consecutive metrics.

11. (Canceled)

12. (Previously presented) The method as claimed in claim 10, further comprising performing the calculation with ACS banks made up of several ACS units.

13. (Previously presented) The method as claimed in claim 12, further comprising connecting the ACS banks used in the calculation in a cascade.

14. (Previously presented) The method as claimed in claim 12, further comprising connecting the ACS banks used in the calculation in parallel.

15. (Previously presented) The method as claimed in claim 12, further comprising performing the decoding by program.

16. (Previously presented) The method as claimed in claim 15, further comprising storing the calculated metrics in a register and reading the metrics of the previous stage from the register when the next stage of the trellis is calculated.

17. (Previously presented) The method as claimed in claim 10, further comprising

a) reading a set of metrics from a memory as inputs to the ACS units,

b) performing the calculation of the metrics of the next stage of the trellis in the ACS units,

c) taking the obtained metrics from the outputs of the ACS units to the inputs of the ACS units for calculating the next stage of the trellis, repeating steps b) and c) one or more times.

18. (Previously presented) The method as claimed in claim 17, further comprising repeating the steps b) and c) until $\log_Y P$ path metrics are calculated, wherein P is the number of data paths and Y is the number of branches from/to a state.

19. (Currently amended) An arrangement for calculating a trellis, wherein the arrangement comprises one or more Add, Compare, Select ("ACS") units, and wherein connections between the inputs and outputs of the ACS units are implemented in such a manner that in calculating consecutive metrics of the trellis, the calculated metrics of the previous stage of

the trellis obtained from the outputs of the ACS units are directly connected to the inputs of the ACS units to be used in the calculation of the next stage of the trellis and the arrangement further comprises a memory for storing the calculation results and that the connection between the inputs and outputs of the ACS units are implemented in such a manner that $\log_Y P$ path metrics are calculated per one memory read/write operation pair, wherein P is the number of data paths and Y is the number of branches from/to a state.